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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:	)
	) Examiner:
Martin Raymond Scott, et al.	)
	) Art Unit: 2631
Application No.: 10/646,087	)
	)
Filed: August 22, 2003	)
	)
For: ADAPTIVE CLOCK RECOVERY	)
	)

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Sir:

Applicants hereby enclose a certified copy of the priority document for the above-referenced patent application. The enclosed document is a certified copy of British Application No. GB 0219786.1, filed August 22, 2003.

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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: ___January 16, 2004___

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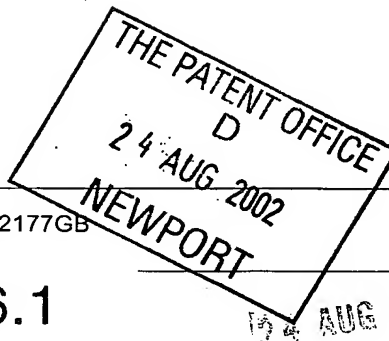
1.	Your reference	JPA.P52177GB
2.	Patent application number *(The Patent Office will fill in this pa*	**0219786.1**
3.	Full name, address and postcode of the or of each applicant *(underline all surnames)*	Zarlink Semiconductor Limited Cheney Manor Swindon Wiltshire SN2 2QW
	Patents ADP number *(if you know it)*	
	If the applicant is a corporate body, give the country/state of its incorporation	United Kingdom
4.	Title of the invention	Adaptive Clock Recovery

S242965001

5.	Name of your agent *(if you have one)*	Marks & Clerk
	"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	4220 Nash Court Oxford Business Park South Oxford OX4 2RU United Kingdom 7271125001
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		Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*
6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number			

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8.	Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:* a) *any applicant named in part 3 is not an inventor, or* b) *there is an inventor who is not named as an applicant, or* c) *any named applicant is a corporate body.* *See note (d))*	Yes

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Description	8
Claim(s)	2
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Priority documents

Translations of priority documents

Statement of inventorship and right
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Request for preliminary examination
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Request for substantive examination
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Any other documents
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11.   I/We request the grant of a patent on the basis of this application.

Signature *Marks & Clerk*   Date 23/08/02

Marks & Clerk   23 August 2002

12. Name and daytime telephone number of   Julian Asquith - 01865 397900
person to contact in the United Kingdom

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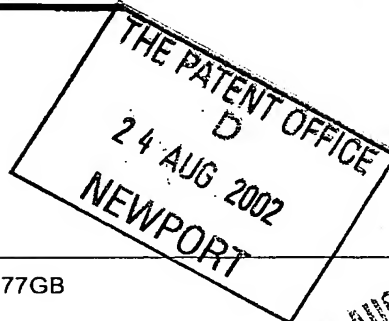
1. Your reference   JPA.P52177GB

2. Patent application numbe
   (if you know it)   **0219786.1**

3. Full name of the or of each applicant
   Zarlink Semiconductor Limited

4. Title of the invention
   Adaptive Clock Recovery

5. State how the applicant *(s)* derived the right
   from the inventor *(s)* to be granted a patent
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7.   I/We believe that the person *(s)* named over the page *(and on any extra copies of this form)* is/are the inventor *(s)* of the invention which the above patent application relates to.

   Signature *Marks & Clark*   Date 23/08/02
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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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Reminder

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Adaptive Clock Recovery

The invention relates to the recovery of clock signals for a TDM output from packets of TDM data which have been transmitted over a packet network.

TDM links are synchronous circuits, with a constant bit rate governed by the service clock $f_{service}$. With a packet network the connection between the ingress and egress frequency is broken, since packets are discontinuous in time. From Figure 1, the TDM service frequency $f_{service}$ at the customer premises must be exactly reproduced at the egress of the packet network (f_{regen}). The consequence of a long-term mismatch in frequency is that the queue at the egress of the packet network will either fill up or empty, depending on whether the regenerated clock is slower or faster than the original. This will cause loss of data and degradation of the service.

The relevant standards on circuit emulation services over ATM, ITU standard I.363.1 and ATM Forum standard af-vtoa-0078 refer to the concept of adaptive clock recovery in general terms.

According to the invention there is provided a method of recovering a clock signal, and a clock recovery system, as set out in the accompanying claims.

Embodiments of the invention will now be more particularly described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram showing a leased line TDM service being carried across a packet network; and

Figure 2 is a schematic diagram showing a clock recovery method based on Transit Time in accordance with an embodiment of the invention.

In Figure 1, the rate of transmission of packets from the source device is isochronous and determined by $f_{service}$. However, the rate of packet arrival at the destination device is

perturbed by the intervening packet network. Packets will typically arrive in bursts separated by varying amounts of delay. The delay between successive packets and bursts will vary depending on the amount of traffic in the network. The characteristics of the network are non-deterministic, but over the long term the rate of arrival at the destination will equal the rate of departure at the source (assuming no lost or duplicate packets).

The TDM output at the destination is isochronous and determined by f_{regen}. This is provided by the Digitally Controlled Oscillator (DCO) (22) in Figure 2. The output is supplied from a Packet Delay Variation (PDV) Buffer (12). If the buffer has zero packets in it when the TDM output requires to transmit then an underrun will occur, which is undesirable. In order to minimise underrun events it is necessary to build up the PDV buffer (12) so that it contains sufficient packets to supply the TDM output for the majority of inter packet delays. However, the PDV buffer (12) cannot be made arbitrarily large because this directly increases the end to end latency which, in general, is required to be as low as possible, the maximum tolerable latency being dependent on the application. For example, voice requires lower latency than data.

Thus the optimal PDV Buffer depth depends upon network conditions and application. The clock recovery method described here allows the buffer depth to be varied independently of the clock recovery mechanism. This allows the clock recovery to stabilise prior to setting up the PDV Buffer, and allows the buffer to be changed during operation to match any underlying shift in network characteristics.

When a packet arrives at the Packet Input (10) it is placed into a PDV Buffer (12) in a Queue (14). It also has its timestamp extracted and passed to a Differencer (16). The Remote timestamp is determined, at the source device when the packet is created, by the source TDM clock $f_{service}$ shown in Figure 1. The Local Timestamp is determined, when the packet is received, by the destination TDM clock f_{regen} also shown in Figure 1.

The Differencer (16) subtracts the Remote Timestamp from the Local Timestamp to obtain the Transit Time.

$$\text{Transit Time (n)} = \text{Local Timestamp(n)} - \text{Remote Timestamp(n)}$$

Equation (1)

It should be noted that because the Local and Remote clock frequencies and initial counts are not initially synchronised with respect to each other, the quantity "Transit Time" in Equation 1 does not represent the actual time that the packet has taken to travel between the source and destination but is instead a measure of the difference between counts of the bit clock cycles of the two clocks.

Hence, given an ideal fixed delay packet network, the Transit Time value will decrease if $f_{service}$ exceeds f_{regen}, will increase if f_{regen} exceeds $f_{service}$, and will remain constant if the frequencies are identical.

For each received packet (assuming no lost packets), the Remote Timestamp will increase by a fixed amount which represents the number of bit clock cycles at the source that have elapsed since the previous packet i.e. the number of bits contained in the packet payload.

This system is robust in the presence of lost packets because the remote and local timestamps of the next packet received following the lost packet(s) are unaffected by the loss. The lost packets merely represent a short term loss of resolution in the measurement. In a typical system there will be thousands of packets per second so that a packet loss rate which is at the maximum likely to occur (i.e. a few percent) will have a negligible effect on the algorithm.

The Timestamps are counts (rather than actual times) that can be thought of as the phase of the clock.

So Equation (1) above can be represented as:

$$\Phi(n) = \theta_2(n) - \theta_1(n)$$

Where:

$\Phi(n)$ is the Transit Time

θ_2 is the phase of the Local Clock in bit periods

θ_1 is the phase of the Remote Clock in bit periods

An indication of the frequency difference, can be obtained:

$$\Delta\Phi(n) = \Phi(n) - \Phi(n-1)$$
$$= [\theta_2(n) - \theta_1(n)] - [\theta_2(n-1) - \theta_1(n-1)]$$
$$= [\theta_2(n) - \theta_2(n-1)] - [\theta_1(n) - \theta_1(n-1)]$$
$$= [f_2(n) - f_1(n)].\,\Delta t$$
$$= \Delta f.\,\Delta t$$

Where

Δt is the interval between packet arrivals.

f1 is the Remote clock frequency

f2 is the Local clock frequency

Δf is the difference between the local and remote clock frequencies

Δf may be used by a Clock Control Algorithm (20) to adjust the Local Clock frequency.

With a real network the Transit Time, $\Phi(n)$, fluctuates due to the burst nature of the incoming packet stream. This causes fluctuations in the recovered clock. Therefore a filter function (24) is provided, which provides the following benefits:

- reduces the workload of the Clock Control Algorithm (20) (which may be implemented by an external CPU) in terms of numerical processing
- reduces the workload of the Clock Control Algorithm (20) by allowing the Clock Control Interval to be increased
- reduces fluctuations in the recovered clock

For example, the filter (24) may be a first order low pass filter with the following difference equation that is simple to implement in hardware without requiring any dividers or multipliers:

$$\Phi_{av}(n) = \Phi_{av}(n-1) + (\Phi(n) - \Phi_{av}(n-1))/2^P \qquad \qquad \textit{Equation (2)}$$

Where:

Φ_{av} is the Filter Output

Φ is the Difference value

P is a programmable parameter that determines the time constant of the filter

n is the sample number that increments each time that a packet is received at the Packet Input

The Clock Control Algorithm (20) can read Φ_{av} at a fixed interval, to obtain

$$\Delta\Phi_{av}(m) = \Phi_{av}(m) - \Phi_{av}(m-1)$$

It can be shown that

$$\Phi_{av}(m) = \theta_{2\,av}(m) - \theta_{1\,av}(m)$$

Where $\theta_{2\,av}(m)$ and $\theta_{1\,av}(m)$ are also obtained by the filtering as described by Equation (2)

Therefore

$$\Delta\Phi_{av}(m) = [\theta_{2\,av}(m) - \theta_{2\,av}(m-1)] - [\theta_{1\,av}(m) - \theta_{1\,av}(m-1)]$$
$$\Delta\Phi_{av}(m) = [f_2(m) - f_1(m-1)].\,\Delta t$$
$$= \Delta f.\,\Delta t$$

Where

Δt is the interval between samples (m) and (m-1).

f1 is the Remote clock frequency

f2 is the Local clock frequency

Δf is the difference between the local and remote clock frequencies

The Clock Control Algorithm (20) will read Φ_{av} and determine the correction required to converge the Local clock to the Remote clock, and write the required Frequency to a DCO (22).

A simple first order Clock Control Algorithm is given by the following difference equation:

$$F(m) = F(m-1) + \beta \ (\Delta\Phi_{av}(m) \ / \ \Delta t)$$

Where:

F(m) is the Frequency to be written to the DCO

F(m-1) is the Current DCO Frequency

β is a constant that determines the time constant

m is the sample number that increments each time the Clock Control Algorithm reads the $\Delta\Phi_{av}$

Δt is the time interval between reads

The time constant is selected to track long term drift in $f_{service}$ but reject short term variation due to packet delay variations.

A PDV Depth Control Algorithm (26) makes relatively infrequent adjustments to the PDV Buffer (12) (by adding or removing packets to or from the buffer) which may be based on :

- Filtered Depth reading of queue depth provided by filter (28), which may be of the type described by Equation (2)
- Underrun events (indicating the Queue (14) is too small)
- Maximum and Minimum Depth readings
- Network Delay Measurements (For example obtained by network "ping" utility)

The Minimum & Maximum depth values are reset to the current Queue Depth each time they are read by the PDV Buffer Depth Control Algorithm (26), and are then adjusted whenever the Packet Queue Depth is altered.

Alternative Filter algorithms may be used.

Alternative Clock Control Algorithms may be used e.g. 2nd and higher order, fuzzy logic, neural networks, and self-tuning algorithms that vary parameters such as the time constant or Clock Control Interval over time.

An internal or external CPU may be used for the Clock Control & Depth Control Algorithms

Byte, frame or packet counts may be used as the Timestamp instead of bits.

The method as described makes use of all the data packets. It is also possible to use a subset of the packets, or to use special timing packets.

It would be possible to implement the method without timestamps where packets are of a consistent payload size.

The method has application in timing recovery over packet based systems or other asynchronous systems. A typical application of the method described above is in emulation of TDM (time division multiplexed) circuits across a packet network, such as Ethernet, ATM or IP. Circuit emulation may be used to support the provision of leased line services to customers using legacy TDM equipment. For example, Figure 1 shows a leased line TDM service being carried across a packet network. The advantages are that a carrier can upgrade to a packet switched network, whilst still maintaining their existing TDM business.

The clock recovery method described above provides the following advantages:

1. The method is able to make use of all of the incoming data packets at the destination device to converge average f_{regen} (i.e. local clock) to average $f_{service}$ (i.e. remote clock).

2. No expensive Clock Generation Circuits are required (such as oven controlled crystal oscillators).

3. Timestamps contained in the incoming packets are compared to a Local Timestamp value to obtain a Transit Time value.

4. The sequence of Transit Time values that is obtained are filtered.

5. The filtered Transit Time value is used by a Clock Control Algorithm to adjust the Local TDM Clock of the device.

6. The separation of the filter from the Clock Recovery Algorithm allows the Clock Control Algorithm to operate at a much slower rate than the filter. So that, for example, a high speed filter could be implemented in Hardware and a low speed Clock Control Algorithm with an external CPU. This confers significant benefits, such as flexibility, reduction of development risk, ease of optimising the solution for a specific environment etc.

7. A method is provided to enable the Local Timestamp to be initialised to the value of the first received Remote Timestamp to minimise wraparound problems and prevent a start up error with the recovered clock.

8. A method is provided to allow packets to be deleted from the PDV Buffer and dummy packets to be inserted into the PDV Buffer in order to adjust the device latency. This does not affect the Local Timestamp value mentioned above.

9. The PDV Buffer Depth is filtered at an appropriate interval.

10. Minimum & Maximum PDV Buffer Depth values are maintained

11. The filtered PDV Buffer Depth, and Minimum & Maximum PDV Buffer Depth values may be used by a Buffer Depth Control Algorithm which may run at a much slower rate than the rate at which the filter is updating.

12. The clock recovery method described here allows the PDV Buffer depth to be varied independently of the clock recovery mechanism. This allows the clock recovery to stabilise prior to setting up the PDV Buffer, and allows the buffer to be changed during operation to match any underlying shift in network characteristics.

CLAIMS:

1.   A method of recovering a clock signal for a TDM output from packets of TDM data which have been transmitted over a packet network, from a source having a source TDM clock to a destination having a destination TDM clock, the method comprising:

providing at least some packets with a Remote Timestamp representing the state of the source TDM clock when the packet is created;

providing said at least some packets with a Local Timestamp representing the state of the destination TDM clock when the packet is received;

determining a Transit Time value representing the difference between said Local and Remote Timestamps; and

controlling the clock frequency of the TDM output on the basis of said Transit Time as determined above.

2.   A method as claimed in claim 1, wherein said Timestamps are based on bit counts at the source and destination TDM clocks.

3.   A method as claimed in claim 1 or 2, wherein a filter is provided to filter said Transit Time value over time.

4.   A method as claimed in claim 3, wherein said filter is a first order low pass filter.

5.   A method as claimed in any preceding claim, wherein received packets are placed in a packet buffer, and the buffer depth is controlled by a depth control algorithm.

6.   A method as claimed in claim 5, wherein said depth control algorithm makes adjustments to said packet buffer by adding or removing packets.

7.   A clock recovery system for recovering a clock signal for a TDM output from packets of TDM data which have been transmitted over a packet network, from a source

having a source TDM clock to a destination having a destination TDM clock, the system comprising:

remote timestamp extraction means for extracting a Remote Timestamp value from received packets, the Remote Timestamp representing the state of the source TDM clock when the packet is created;

local timestamp means for providing received packets with a Local Timestamp representing the state of the destination TDM clock when the packet is received;

a differencer for determining the difference between said Local and Remote Timestamps; and

clock control means arranged to control the frequency of the TDM output on the basis of said difference value.

8.   A clock recovery system as claimed in claim 7, wherein said Timestamps are based on bit counts at the source and destination TDM clocks.

9.   A clock recovery system as claimed in claim 7 or 8, which further comprises a filter for filtering the output of said differencer.

10.   A clock recovery system as claimed in claim 9, wherein said filter is a first order low pass filter.

11.   A clock recovery system as claimed in any of claims 7 to 10, which further comprises a packet buffer for holding received packets, and a depth control arrangement for controlling the depth of the packet buffer.

12.   A clock recovery system as claimed in claim 11, wherein said depth control arrangement is arranged to make adjustments to said packet buffer by adding or removing packets.

ABSTRACT

Adaptive Clock Recovery

A method of recovering a clock signal for a TDM output from packets of TDM data which have been transmitted over a packet network, from a source having a source TDM clock to a destination having a destination TDM clock, comprises:

providing at least some packets with a Remote Timestamp representing the state of the source TDM clock when the packet is created;

providing said at least some packets with a Local Timestamp representing the state of the destination TDM clock when the packet is received;

determining a Transit Time value representing the difference between said Local and Remote Timestamps; and

controlling the clock frequency of the TDM output on the basis of said Transit Time as determined above.
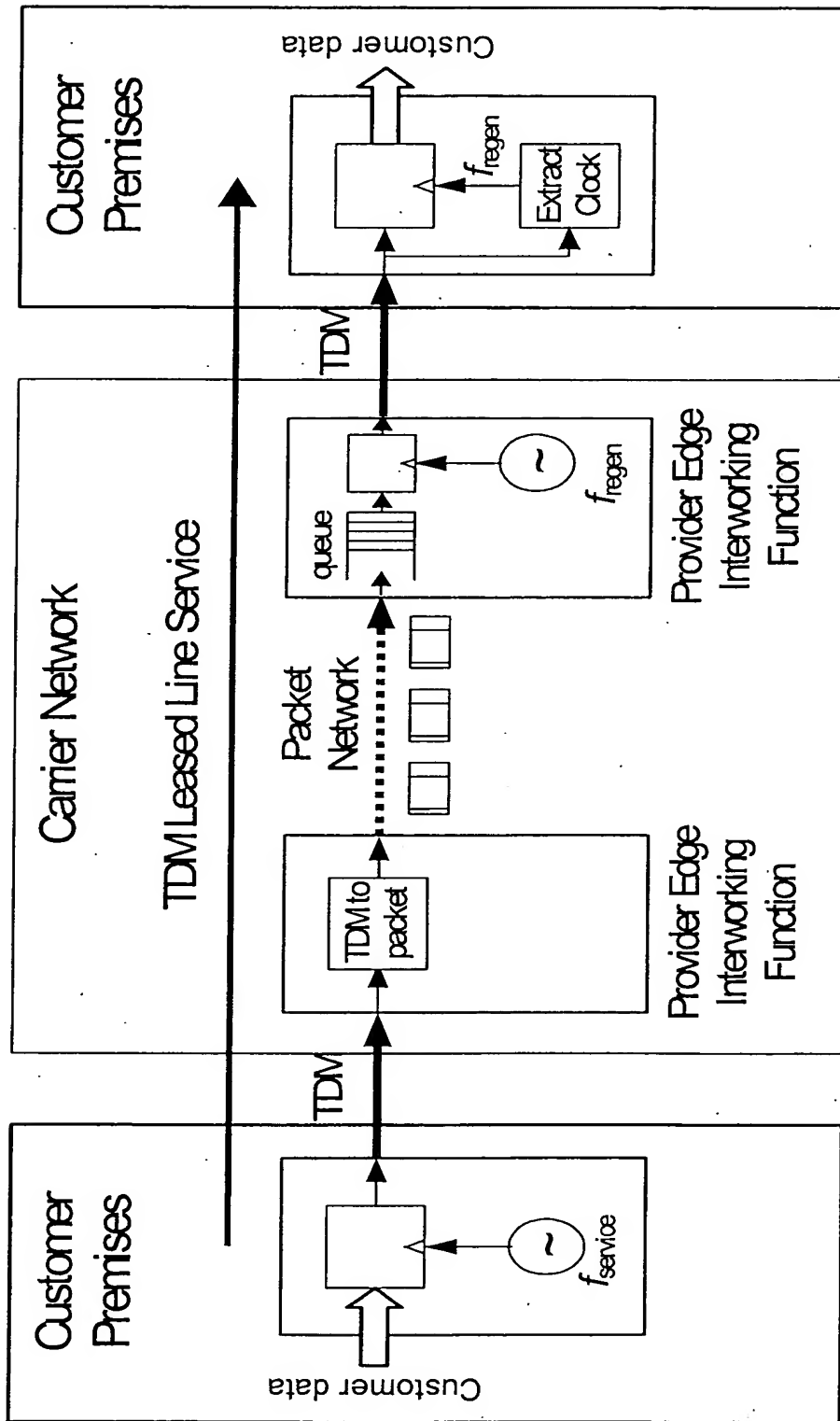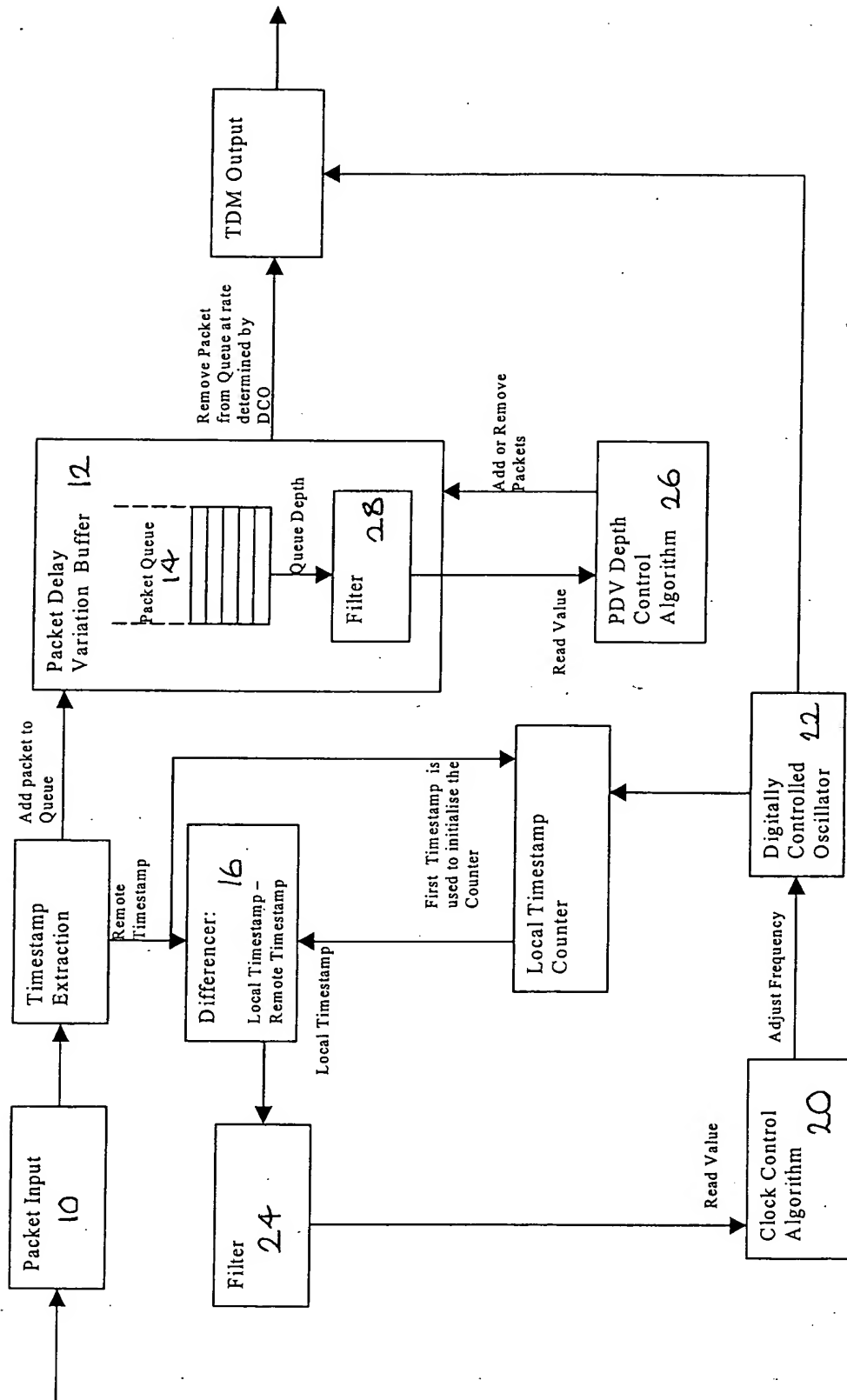
Refer to Figure 2.

Figure 1

Figure 2